Exhibit A

As of February 2008.

MICHEL DUBOIS

IEEE Fellow (1999)
ACM Fellow (2005)

Professor of Computer Engineering
Department of Electrical Engineering
University of Southern California
Los Angeles, CA 90089-2562
(213)-740-4475
dubois@paris.usc.edu

A. Employment History

- Professor of Electrical Engineering, University of Southern California, Los Angeles, California; on the faculty since September 1984.
- Research Engineer, Central Research Laboratory of Thomson-CSF, Orsay, France, from March 1982 to August 1984. In an advanced development group in computer architecture.

B. Education

- Purdue University: 1978-82. Ph. D. in Electrical Engineering. General areas of research: computer architecture, performance evaluation applied to architecture design, and architectures for digital image processing.
- University of Minnesota: 1976-78. M.S. in Electrical Engineering. General area of research: digital signal and image processing.
- Faculte Polytechnique de Mons (Belgium): 1971-76. Degrees in Electrical Engineering and Nuclear Engineering.

C. Major Research Accomplishments

- Has published more than 100 technical papers on computer architecture and algorithms. Nine of these papers were published in the International Symposium on Computer Architecture, a premier conference in computer architecture.
- Is well-known in the field of architecture (and well referenced in the literature) for his early contributions (with Christoph Scheurich) to the problem of coherence, synchronization and memory access order in shared-memory multiprocessors.
- Has developed (with Fong Pong) a new approach for the verification of coherence protocols based on abstraction. Protocols can be verified rapidly at various stages of development and for any system size.
- Has conceived and evaluated various latency tolerance mechanisms for shared-memory multiprocessors using execution-driven simulations. In particular, he developed during his sabbatical at Lund University in Sweden a new algorithm to classify misses and updates based on values communicated among processors.
- Has built with his PhD students and under NSF funding a working, general-purpose hardware multiprocessor emulator with FPGAs, which can be used to build rapid and cost-effective hardware prototypes of multiprocessor systems.

D. Publications

(1) Journal Papers (published and accepted)

[1] Y. Yasuda, M. Dubois, and T.S. Huang, "Data Compression for Check Processing Machines," Proceedings of the IEEE, July 1980, pp. 874-885.

[2] M. Dubois and F.A. Briggs, "Performance of Synchronized Iterative Processes in Multiprocessors," IEEE Transactions on Software, July 1982, pp. 419-431.

[3] M. Dubois and F.A. Briggs, "Effects of Cache Coherency in Multiprocessors," IEEE Transactions on Computers, C-31, No. 11, Nov. 1982, pp. 1083-1099.

[4] F.A. Briggs and M. Dubois, "Effectiveness of Private Caches in Multiprocessor Systems with Parallel-Pipelined Memories," IEEE Transactions on Computers, C-32, No. 1, January 1983, pp. 48-59.

[5] M. Dubois, "A Cache-based Multiprocessor with High Efficiency," IEEE Transactions on Computers, October 1985, pp. 968-972.

[6] J.L. Gaudiot, M. Dubois, L.T. Lee, and N. Tohme, "The TX-16: A Highly Programmable Multimicroprocessor Architecture," IEEE Micro, October 1986, pp. 18-31.

[7] M. Dubois, "Throughput Analysis of Cache-based Multiprocessors with Multiple Buses," IEEE Transactions on Computers, Jan. 1988, pp. 58-70.

[8] M. Dubois, C. Scheurich, and F.A. Briggs, "Synchronization, Coherence and Ordering of Events in Multiprocessors," IEEE Computer, Feb. 1988, pp. 9-21.

[9] A. Uresin and M. Dubois, "Sufficient Conditions for the Convergence of Asynchronous Iterations," Parallel Computing, 10, March 1989, pp. 83-92.

[10] M. Dubois and S. Thakkar, "Cache Architectures in Tightly-Coupled Multiprocessors," Guest Editors' Introduction, Special Issue of IEEE Computer, Vol. 23, No. 6, June 1990, pp. 9-11.

[11] S. Thakkar, M. Dubois, "Scalable Shared-Memory Multiprocessor Architectures," Special Issue of IEEE Computer, Vol. 23, No. 6, June 1990, pp. 71-74.

[12] C. Scheurich and M. Dubois, "Dynamic Page Migration in Multiprocessors with Distributed Global Memory," IEEE Transactions on Computers, Special Issue on Distributed Computer Systems, August 1989, pp. 1154-1163.

[13] M. Dubois, and C. Scheurich, "Memory-Access Dependencies in Shared-memory Multiprocessors," IEEE Transactions on Software Engineering, Vol. 16, No. 6, June 1990, pp. 660-673.

[14] A. Uresin and M. Dubois, "Parallel Asynchronous Algorithms for Discrete Data," Journal of the Association for Computing Machinery (JACM), Vol.37, No. 3, July 1990, pp. 588-606.

[15] J-C Wang and M. Dubois, "A Performance Comparison of Cache Coherence Protocols Based on the Access-Burst Model," Computer Systems Science and Engineering, Vol. 5, No. 3, July 1990, pp. 147-158.

[16] C. Scheurich and M. Dubois, "Lockup-free Caches in High-Performance Multiprocessors," Journal of Parallel and Distributed Computing, 11, 25-36, January 1991.

[17] M. Dubois and J-C Wang, "Shared Data Contention in a Cache Coherence Protocol," IEEE Transactions on Computers, Vol. 40, No 5, pp. 640-645, May 1991.

[18] M. Dubois and F.A. Briggs, "The Runtime Efficiency of Parallel Asynchronous Algorithms," IEEE Transactions on Computers, Vol. 40, No. 11, pp. 1260-1266, Nov. 1991.

[19] M. Dubois and S. Thakkar, “Special Issue on Memory System Architectures for Scalable Multiprocessors--Guest Editors' Introduction", Journal of Parallel and Distributed Computing, August 1992, pp. 303-304.

[20] L. Barroso, S. Iman, J. Jeong, K. Oner, K. Ramamurthy and M. Dubois, “RPM: A Rapid Prototyping Engine for Multiprocessor Systems,” IEEE Computer, pp. 26-34, February 1995.

[21] L. Barroso and M. Dubois, “Performance of the Slotted-Ring Multiprocessor,” IEEE Transactions on Computers, pp. 878-890, July 1995.

[22] F. Dahlgren, M. Dubois and P. Stenstrom, “Fixed and Adaptive Sequential Prefetching in Shared-Memory Multiprocessors,” IEEE Transactions on Parallel and Distributed Systems, Vol. 6, No. 7, pp. 733-746, July 1995.

[23] H. Nilsson, P. Stenstrom and M. Dubois, “Implementation and Evaluation of Update-Based Cache Protocols Under Relaxed Memory Consistency Models,” Journal of Future Generation Computer Systems, 11(3):247-271, June 1995.

[24] F. Pong and M. Dubois, “A New Approach for the Verification of Cache Coherence Protocols,” IEEE Transactions on Parallel and Distributed Systems, Vol. 6, No. 8, pp. 773-787, August 1995.

[25] M. Dubois, J. Skeppstedt, and P. Stenstrom, “Essential Misses and Data Traffic in Multiprocessors,” Journal of Parallel and Distributed Computing, Vol. 29, No. 2, pp. 108-125, September 1995.

[26] A. Uresin and M. Dubois, “Effects of Asynchronism on the Convergence of a Class of Iterations,” Journal of Parallel and Distributed Computing, 34, pp. 66-81, April 1996.

[27] P. Stenstrom, M. Brorrson, F. Dahlgren, H. Grahn, and M. Dubois,”Boosting Multiprocessor Program Performance Using Optimized Cache Coherence Protocols,” IEEE Computer, Vol. 30, No. 7, pp. 63-70, July 1997.

[28] F. Pong and M. Dubois, “Verification Techniques for Cache Coherence Protocols,” ACM Surveys, Vol. 29, No. 1, pp. 82-126, March 1997.

[29] M. Cekleov and M. Dubois, “Virtual-address Caches, Part I: Problems and Solutions in Uniprocessors,” IEEE Micro, Vol. 17, No 5, pp.64-71, September/ October 1997.

[30] M. Cekleov and M. Dubois, “Virtual-address Caches, Part II: Multiprocessor Issues,” IEEE Micro, Vol. 17, No. 6, pp. 69-74, November/December 1997.

[31] F. Pong, M. Browne, G. Aybay, A. Nowatzyk, and M. Dubois,"Design Verification of the S3.mp Cache-Coherent Shared-Memory System," IEEE Transactions on Computers, Vol. 47, No. 1, pp.135-140, Jan. 1998.

[32] F. Pong and M. Dubois, “Formal Verification of Complex Coherence Protocols Using Symbolic State Models,” Journal of the ACM (JACM), pp. 557-587, July 1998.

[33] K. Lee and M. Dubois, “Empirical Models of Miss Rates,” Parallel Computing, No. 24, pp. 205-219, 1998.

[34] M. Dubois, J. Jeong, Y.H. Song, and A. Moga, "Rapid Prototyping on RPM-2: Methodology and Experience," IEEE Design and Test of Computers, pp. 112-118, July-September 1998.

[35] F. Dahlgren, P. Stenstrom and M. Dubois, “Performance Evaluation and Cost Analysis of Cache Protocol Extensions for Shared-Memory Multiprocessors,” IEEE Transactions on Computers, Vol. 47, No. 10, pp. 1041-1056, October 1998.

[36] W-J Hahn, S-H Yoon, K. Lee, and M. Dubois,"Evaluation of a Cluster-based System for OLTP Applications," ETRI Journal, Vol. 20, No. 4, pp. 301-326, December 1998.

[37] J-C Wang, J. Chame and M. Dubois, “Modeling Finite Cache Effects in Write-invalidate snooping protocols” International Journal of Computer Systems Science & Engineering, Vol. 14, No. 1, January 1999.

[38] J. Skeppstedt and M. Dubois,"Hybrid prefetching in Multiprocessors," Journal of Parallel and Distributed Computing (JPDC), Vol. 60, No 5, pp.585-615, May 2000.

[39] F. Pong and M. Dubois,“A Verification Framework for Delayed Consistency Protocols Based on a Symbolic State Model," IEEE Transactions on Parallel and Distributed Systems, Vol. 11, No. 9, pp. 989-1006, Sept. 2000.

[40] M. Dubois, J. Jeong, and A. Nanda,"Shared-Cache Architectures for Decision-Support Systems," International Journal of Performance Evaluation, Vol. 49, September 2002, pp. 283-298.

[41] A. Moga and M. Dubois "Scalability Implications of Software-implemented Coherence," International Journal of Computer Systems Scienec & Engineering, Vol. 18, No. 1, Januray 2003, pp. 7-16.

[42] Xiaogang Qiu and Michel Dubois,"Tolerating Late Memory Traps in Dynamically-scheduled Processors," IEEE Transcations on Computers, June 2004, Vol. 53, No.6, pp.732-743.

[43] Xiaogang Qiu and Michel Dubois,"Moving Address Translation Closer to Memory in Distributed Shared Memory Multiprocessors," IEEE Transactions on Parallel and Distributed Systems, July 2005, 16, No 7, pp. 612-623.

[44] J. Jeong and M. Dubois,"Cache Replacement Algorithms with Nonuniform Miss Costs," IEEE Transactions on Computers, Vol. 55, No. 4, April 2006, pp. 353-365.

[45] J. Chen, P. Stenstrom and M. Dubois, "Integrating Complete-system and User-level Performance/Power Simulators: the SimWattch Approach," IEEE Micro, pp. 34-48, July 2007.

[46] W. Choi and M. Dubois,"Accurate Instruction Pre-scheduling in Dyanamically Scheduled Processors," Transactions on High-Performance Embedded Architectures and Compilers, 2(2):1-18, April 2007.

[47] J. Jeong, Per Stenstrom and M. Dubois,"Simple Penalty-Sensitive Replacement Policies for Caches," accepted Journal of Instruction-Level Parallelism (JILP), December 2007.

(2) Journal Papers (submitted)

[48] A. Moga and M. Dubois, "A Comparative Evaluation of hybrid Distributed Shared-memory Systems" submitted to the Journal on Systems Architecture, August 2006, minor revision in progress.

[49] X. Qiu and M. Dubois,"The Synonym Lookaside Buffer: A Solution to the Synonym Problem in Virtual Caches," submitted to IEEE Transactions on Computers, September 2006, Major revision in progress.

[50] J. Chen, P. Stenstrom and M. Dubois, "SimWattch: Integrating Complete-system and User-level Performance and Power Simulators," Invited to IEEE Potentials.

(3) Books

[1] Cache and Interconnect Architectures in Multiprocessors. Edited by M. Dubois and S. Thakkar, Kluwer Academic Publishers, 1990.

[2] Scalable Shared-Memory Multiprocessors. Edited by M. Dubois and S. Thakkar, Kluwer

Academic Publishers, 1991.

(4) Chapters in Books

[1] A. Uresin and M. Dubois,"Asynchronous Iterative Algorithms: Models and Convergence," in Advances in Parallel Algorithms, Chapter 11, Edited by L. Kronsjo, Blackwell Scientific Publications, 1992.

[2] M. Dubois, "Multiprocessing and Multitasking," in Encyclopedia of Microcomputers, Vol. 11, Marcel Dekker, Inc., 1993.

[3] J. Jeong, R. Sahoo, K. Sugavanan, A. Nanda, and M. Dubois,"Evaluation of Large L3 Caches Using TPC-H Trace samples," Chapter 7 in "High-Performance Memory Systems," edited by H. Hadimioglu et al., Springer, 2003.

(5) Conference Proceedings

[1] F.A. Briggs and M. Dubois, "Modeling of Synchronized Iterative Algorithms for Multiprocessors, " Proceedings of the 18th Annual Allerton Conference, October 1980, pp. 554-563.

[2] F.A. Briggs, M. Dubois, and K. Hwang, "Throughput Analysis and Configuration Design of a Shared-Resource Multiprocessor System: PUMPS," Proceedings of the 8th International Symposium on Computer Architecture, May 1981, pp. 67-79.

[3] M. Dubois and F.A. Briggs, "Efficient Interprocessor Communication for MIMD Multiprocessor Systems," Proceedings of the 8th International Symposium on Computer Architecture, May 1981, pp. 187-196.

[4] K. Hwang, F.A. Briggs, M. Dubois, and K.S. Fu, "PUMPS Architecture for Pattern Analysis and Image Database Management," Proceedings of the IEEE Pattern Recognition and Image Processing Conference, August 1981.

[5] F.A. Briggs and M. Dubois, "Cache Effectiveness in Multiprocessor Systems with Parallel-Pipelined Memories," Proceedings of the 1981 International Conference on Parallel Processing, August 1981, pp. 306-313.

[6] F.A. Briggs and M. Dubois, "Performance of Cache-Based Multiprocessors," ACM Conference on Measurement and Modeling of Computer Systems, September 1981, pp. 181-190.

[7] M. Dubois and F.A. Briggs, "Effects of Cache Coherency in Multiprocessors," Proceedings of the 9th Annual Symposium on Computer Architecture, April 1982, pp. 299-310.

[8] M. Dubois and F.A. Briggs, "An Approximate Analytical Model for Asynchronous Processes in Multiprocessors," Proceedings of the 1982 Parallel Processing Conference, Aug. 1982, pp. 290-297.

[9] M. Dubois, "Performance Evaluation of the SCQM Multiprocessor System," (in French) 2nd International Conference on Performance Analysis Tools and Methodologies, Paris, May 1984.

[10] J-L Gaudiot and M. Dubois, "An Integrated Solution To Large-Scale Computing Problems," International Symposium on New Directions in Computing, Trondheim, Norway, August 1985.

[11] M. Dubois, "A Cache-based Multiprocessor with High Efficiency," International Conference on Parallel Processing, August 1985, pp. 646-648.

[12] M. Dubois, C. Scheurich, and F.A. Briggs, "Memory Access Buffering in Multiprocessors," Proceedings of the 13th International Symposium on Computer Architecture, June 1986, Tokyo, Japan, pp. 434-442.

[13] M. Dubois, F.A. Briggs, I. Patil, and M. Balakrishnan, “Trace-driven Simulations of Parallel and Distributed Algorithms in Multiprocessors,” Proceedings of the 1986 International Conference on Parallel Processing, August 1986, pp. 909-916.

[14] A. Uresin and M. Dubois, “Generalized Asynchronous Iterations,” CONPAR'86: Conference on Algorithms and Hardware for Parallel Processing, Springer-Verlag Ed., Sept. 1986, pp. 272-278.

[15] C. Scheurich and M. Dubois, “Dynamic Memory Allocation in a Mesh-connected Multiprocessor,” Proceedings of the 20th Hawaii International Conference on System Sciences, January 1987, pp. 302-311.

[16] M. Balakrishnan, M. Dubois, F.A. Briggs, and I. Patil, “An Efficient Tool for Multiprocessor Systems Simulations,” 4th International symposium on Modelling and Simulation Methodology, Tucson, Arizona, January 1987 (extended abstract).

[17] M. Dubois, “Performance of S.O.R. Algorithms in Modern Multiprocessors,” Proceedings of the 2nd Int. Conference on Supercomputing, Santa Clara, CA, May 1987, pp. 414-423.

[18] C. Scheurich and M. Dubois, “Correct Memory Operation of Cache-based Multiprocessors,” 14th Int. Symposium on Comp. Arch., June 1987, pp. 234-243.

[19] A. Uresin and M. Dubois, “Asynchronous Relaxation for Non-numerical Algorithms,” Int. Conf. on Parallel Processing, August 1987, pp. 499-501.

[20] M. Dubois, “Effect of Invalidations on the Hit Ratio of Cache-based Multiprocessors,” Int. Conf. on Parallel Processing, August 1987, pp.255-257.

[21] J.-C. Wang and M. Dubois, “A Performance Comparison of Cache Coherence Protocols” 2nd Parallel Processing Symposium, April 1988.

[22] C. Scheurich and M. Dubois, “Dynamic Page Migration in Multiprocessors with Distributed Global Memory,” 8th International Conference on Distributed Computing Systems, June 1988.

[23] C. Scheurich and M. Dubois, “Concurrent Miss Resolution in Multiprocessor Caches” 1988 Int. Conf. on Parallel Processing, August 1988.

[24] M. Dubois and J.C. Wang, “Shared Data Contention in a Cache Coherence Protocol” 1988 Int. Conf. on Parallel Processing, August 1988.

[25] C. Scheurich and M. Dubois, “Design of Lockup-free Caches for Multiprocessors” Supercomputing'88, November 1988.

[26] A. Uresin and M. Dubois, “On the Performance of Asynchronous Algorithms,” 3rd Int. Symposium on Computer and Information Sciences, October 1988.

[27] A. Uresin and M. Dubois, “An Asynchronous All Pairs Shortest Path Algorithm for Shared-Memory Multiprocessors,” 26th Annual Allerton Conference on Communication, Control, and Computing, September 1988.

[28] M. Dubois and J-C Wang, “Program Models for Data Sharing and Their Application to Cache-based Multiprocessors,” Int. Computer Symposium, December 1988.

[29] J-C Wang and M. Dubois, “Memory-Access Penalties in Write-Invalidate Cache Coherence Protocols,” Workshop on Cache and Interconnect Architectures in Multiprocessors. Kluwer Academic Publishers, pp. 109-130, June 1989.

[30] M. Cekleov, M. Dubois, J-C Wang and F.A. Briggs. Virtual Address Caches in Multiprocessors. Workshop on Cache and Interconnect Architectures in Multiprocessors. Kluwer

Academic Publishers, pp. 15-35, June 1989.

[31] M. Dubois and S. Thakkar, “Workshop Report: Cache and Interconnect Architectures in Multiprocessors,” Computer Architecture News, Vol. 17, No. 6, December 1989, pp. 105-110.

[32] K. Hwang, M. Dubois, D.K. Panda, S. Rao, S. Shang, A. Uresin, W. Mao, H. Nair, M. Lytwyn, F. Hsieh, J. Liu, S. Mehrotra, and C.M. Cheng. “OMP: A RISC-based Multiprocessor using Orthogonal-Access Memories and Multiple Spanning Buses,” Proceedings of the ACM Supercomputing Conference, June 1990.

[33] A. Economides and M. Dubois “Transient Models of Bus-based Multiprocessors,” Int. Conf. on Parallel Processing, August 1990.

[34] A. Uresin and M. Dubois, “Asynchronous Iterations with Bounded Delay” Int. Conf. on Parallel Processing, August 1990.

[35] S. Mehrotra, C.M. Cheng, M. Dubois, K. Hwang, and D.K. Panda, “Algorithm-driven Simulation and Projected Performance of the USC Orthogonal Multiprocessor,” Int. Conf. on Parallel Processing, August 1990.

[36] J-C Wang and M. Dubois, “Correlation Between Cache Size and Coherence Protocol Overhead,” Proc. of Int. Computer Symposium, pp. 811-814, December 1990.

[37] L. Barroso and M. Dubois, “Cache Coherence on a Slotted Ring,” Int. Conf. on Parallel Processing, pp. I-230-I-237, August 1991.

[38] J-C Wang and M. Dubois, “A Model for Finite Cache Effects,” Int. Conf. on Parallel Processing, August 1991.

[39] M. Dubois, J-C Wang, L. Barroso, K. Lee, and Y-S Chen, “Delayed Consistency and Its Effects on the Miss Rate of Parallel Programs,” Supercomputing'91, Nov. 1991, pp. 197-206.

[40] A. Khokhar and M. Dubois, “Matching Algorithms and Architecture in Hierarchical Shared-Memory Multiprocessor (HSM) Systems,” Int. Par. Proc. Symp., April 1992, pp. 558-561.

[41] M. Dubois, L. Barroso, Y. Chen, and K. Oner, “Scalability Problems in Multiprocessors with Private Caches,” PARLE'92, June 1992, pp. 211-230 (Invited Paper)

[42] M. Dubois, “Delayed Consistency," Workshop on Scalable Shared-Memory Multiprocessors, Kluwer Academic Publishers, December 1992.

[43] Y.-S. Chen and M. Dubois, “Cache Protocols with Partial Block Invalidations,” Int. Par. Proc. Symp., April 1993, pp. 16-23.

[44] J. Chame and M. Dubois, “Cache Inclusion and Processor Sampling in Multiprocessor Simulation,” ACM Sigmetrics Conference on Measurement and Modeling of Computer Systems, May 1993, pp. 36-47.

[45] L. Barroso and M. Dubois, “The Performance of Cache-Coherent Ring-based Multiprocessors,” Int. Symp. on Computer Architecture, May 1993, pp. 268-277.

[46] M. Dubois, J. Skeppstedt, L. Ricciulli, K. Ramamurthy, and P. Stenstrom, “The Detection and Elimination of Useless Misses in Multiprocessors,” Int. Symp. on Computer Architecture, May 1993, pp. 88-97.

[47] F. Pong and M. Dubois, “The Verification of cache Coherence Protocols,” ACM Symposium on Parallel Architectures and Algorithms (SPAA), June 1993, pp. 11-20.

[48] K. Oner and M. Dubois, “Effects of Memory Latencies on Nonblocking Processor/Cache Architectures”, Proceedings of International Conference on Supercomputing, July 1993, pp. 338-

347.

[49] F. Dahlgren, M. Dubois, and P. Stenstrom, “Fixed and Adaptive Sequential Prefetching in Shared Memory Multiprocessors,” Proc. of the Int. Conf. on Parallel Processing, Aug. 1993, pp.I56-I63.

[50] F. Pong and M. Dubois, “Correctness of a Directory-based Cache Coherence Protocol: Early Experience,” Proc. of the 5th IEEE Symposium on Parallel and Distributed Processing, Dec. 1993, pp. 37-44.

[51] F. Dahlgren, M. Dubois, and P. Stenstrom, “Combined Performance Gains of Simple Cache Protocol Extensions,” Int. Symp. on Computer Architecture, April 1994, pp. 187-199.

[52] F. Pong, P. Stenstrom, and M. Dubois, “An Integrated Methodology for the Verification of Directory-based Cache Protocols,” Int. Conf. on Parallel Processing (ICPP), August 1994, pp. I158-I165.

[53] K. Oner, L. Barroso, S. Iman, J. Jeong, K. Ramamurthy, and M. Dubois, “The Design of RPM: An FPGA-based Multiprocessor Emulator,” Proc. 3rd ACM Int. Symposium on Field-Programmable Gate Arrays, Feb. 1995.

[54] F. Pong, A. Nowatzyk, G. Aybay, and M. Dubois, “Verification of S3.mp--A Case Study of Distributed Directory-based Cache Coherence Protocol,” *EUROPAR*’95, pp. 287-300, September 1995.

[55] A. Moga and M. Dubois, “Performance of Asynchronous Linear Iterations with random delays,” Int. Parallel Processing Symposium, IPPS’96, May 1996.

[56] F. Pong and M. Dubois, “Formal Verification of Delayed Consistency Protocols,” Int. Parallel Processing Symposium, IPPS’96, May 1996.

[57] M. Dubois, A. Gefflaut, J. Jeong, A. Moga, and K. Oner,"Rapid Prototyping of Multiprocessor Architectures on RPM: Early Experience," Proceedings of the 5th IFIP Int. Workshop on Logic and Architecture Synthesis, December 1996.

[58] J. Skeppstedt and M. Dubois,"Hybrid Compiler/Hardware Prefetching for Multiprocessors Using Low-Overhead Cache Miss Traps," Int. Conf. on Parallel Processing (ICPP), August 1997, pp. 298-305.

[59] A. Moga and M. Dubois,"Hardware vs Software Implementation of COMA," Int. Conf. on Parallel Processing (ICPP), August 1997, pp. 248-256.

[60] K. Lee, W-J. Han and M. Dubois,"Bottleneck-free Interconnect and I/O Subsystem in SPAX," 1997 Int. Conf. on Parallel and Distributed Systems, Dec. 1997.

[61] A. Moga and M. Dubois,"The Effectiveness of SRAM Network caches in Clustered DSM's," Proc. of the 4th Int. Conf. on High-Performance Computer Architecture (HPCA), pp. 103-112, January 1998.

[62] X. Qiu and M. Dubois, "Options for Dynamic Address Translation in COMAs," 25-th International Symposium on Computer Architecture (ISCA), pp. 214-225, June 1998.

[63] C. Ho, H. Ziegler and M. Dubois, "In-memory Directories: Eliminating the Cost of Directories in CC-NUMAs," Symposium on Parallel Algorithms and Architectures, SPAA’98, pp. 222-230, June 1998.

[64] M. Dubois, C. Scheurich and F.A. Briggs,"Memory Access Buffering in Multiprocessors," reprinted in Selected papers, 25 Years of International Symposia on Computer Architecture, G. Sohi Ed., (includes the 41 most influencial papers from the Int. Symposium on Computer

Architecture (ISCA) since its inception. This selection was made by a committee made of past ISCA program chairs still active. pp. 320-328, June 1998.

[65] M. Dubois and C. Scheurich, "Retrospective on: Memory Access Buffering in Multiprocessors," in Selected papers, 25 Years of International Symposium on Computer Architecture, G. Sohi Ed., pp. 48-50, June 1998.

[66] X. Qiu and M. Dubois, "Tolerating Late Memory Traps in ILP Processors," 26-th International Symposium on Computer Architecture (ISCA), May 1999, pp. 76-87.

[67] J. Jeong and M. Dubois,"Optimal Replacements in Caches with Two Miss Costs," 11th Annual ACM Symposium on Parallel Algorithms and Architectures (SPAA), June 1999, pp.155-164.

[68] A. Moga and M. Dubois,"The Impact of Memory Organization in Hybrid DSMs" 2nd Workshop on Software Distributed Shared Memory, Santa Fe, May 2000.

[69] X. Qiu and M. Dubois, "Towards Virtually-addressed Memory Hierarchies," Proceedings of the 7th Int. Conf. on High-Performance Computer Architecture (HPCA), January 2001,pp.51-62.

[70] J. Jeong, R. Sahoo, K. Sugavanam, A. Nanda, and M. Dubois, "Evaluation of TPC-H Bus Trace Samples Obtained with MemorIES," ISCA 2001 Workshop on Memory Performance Issues, June 2001.

[71] M. Kampe, P. Stenstrom, and M. Dubois,"The FAB Predictor: Using Fourier Analysis to Predict the Outcome of Conditional Branches," Proceedings of the 8th Int. Conf. on High-Performance Computer Architecture (HPCA-8), February 2002,pp.223-232.

[72] M. Dubois, J. Jeong, S. Jahromi, M. Rouhanizadeh, and A. Nanda,"Evaluation of Shared Cache Architectures for TPC-H.," 5th Workshop on Computer Architecture Evaluation using Commercial Workloads, Cambridge, Mass., Feb 2002, pp. 5-12.

[73] J. Jeong and M. Dubois,"Cost-Sensitive Cache Replacement Algorithms," Second Workshop on Caching, Coherence and Consistency, June 2002.

[74] M. Dubois, J. Jeong, and A. Nanda,"Shared-Cache Architectures for Decision-Support Systems," Proceedings of Performance 2002, September 2002, pp. 283-298.

[75] J. Jeong and M. Dubois, " Cost-sensitive Cache Replacement Algorithms," Proceedings of the Symposium on High-Performance Computer Architecture (HPCA), January 2003.

[76] J. Chen, M. Dubois, and P. Stenstrom,"Integrating Complete-System and User-level Performance/Power Simulators: The SimWattch Approach," Proceedings of the 2003 IEEE International Symposium on Performance Analysis of Systems and Software, March 2003.

[77] M. Dubois,"Fighting the Memory Wall with Assisted Execution," 2004 ACM Computing Frontiers Conference, April 2004, pp. 168-180.

[78] M. Kampe, P. Stenstrom, and M. Dubois,"Self-Correcting LRU Replacement policies," 2004 ACM Computing Frontiers Conference, April 2004, pp. 181-191.

[79] N. Moyuddin, R. Bhatti, and M. Dubois, "Controlling Leakage Power with the Replacement Policy in Slumberous Caches," ACM Computing Frontiers Conference, May 2005.

[80] J. Jeong, Per Stenstrom and M. Dubois,"Simple Penalty-Sensitive Replacement Policies for Caches," ACM Computing Frontiers Conference, May 2006.

[81] M. Islam, A. Busck, M. Engbom, S. Lee, M. Dubois, P. Stenstrom,"Limits on Thread-Level Speculative Parallelism in Embedded Applications," 11th Workshop on the interaction between

Compilers and Computer Architecture (INTERACT 11), held in conjunction with HPCA, Feb 2007.

[82] M. Dubois, H. Lee and L. Lin,"STAMP: A Universal Algorithmic Model for Next Generation Multithreaded Machines and Systems," Workshop on Multithreaded Architectures and Applications (MTAAP), held in Conjunction with IPDPS, March 2007.

[83] M. Islam, A. Busck, M. Engbom, S. Lee, M. Dubois, P. Stenstrom, "Loop-level Speculative Parallelism in Embedded Applications," Proc. of the Int. Conference on Parallel Processing, eptember 2007

E. Research Funding

(1) Past

[1] Equipment Grant: Principal Investigator for an NSF Small Equipment Grant, received August 1986, $76,000. (with K. Hwang and J-L Gaudiot).

[2] U.S.C. Faculty Innovation Fund, “Performance Analysis of a Reconfigurable Multiprocessor System,” from July 1, 1985 to July 1, 1986; $18,500 (with J-L Gaudiot)

[3] U.S.C. Faculty Innovation Fund, “A Data-Driven Instruction Pipeline for Supercomputing,” from January 1, 1986 to December 31, 1986; $14,010 (no co-PI).

[4] NSF Grant No. DMC-8505328, “Designing and Programming High-speed Multiprocessors,” Research Initiation Grant from September 1, 1985 to September 1, 1987, $60,000 (no co-PI).

[5] NSF Grant No. DCCR-8709997, “Implementations and Evaluations of Non-Numerical Algorithms for MIMD Multiprocessors,” from November 1987 to November 1990, $175,423 (no co-PI).

[6] AT&T Grant, “Asynchronous Algorithms: Design and Implementations,” from July 1988 to July 1990, $174,000 (no co-PI).

[7] NSF Grant No. CCR-9115725, “An Evaluation of Delayed Consistency Protocols,” from July 1992 to June 1994, $136,545 (no co-PI).

[8] ETRI (Electronics and Telecommunications Research Institute of Korea), “Performance Evaluation of OLTP workloads”, from June 1, 1995 to May 31, 1996, $49,683 (no co-PI).

[9] ETRI (Electronics and Telecommunications Research Institute of Korea), “Evaluation of Future Transaction Processing Systems”, from September 1, 1996 to August 31, 1997, $49,999 (no co-PI).

[10] NSF Grant No. CCR-9222734, “Asynchronous Algorithms: Scalable Algorithms for Multiprocessors” from Sept. 1, 1993 to Aug. 31, 1996 (extended through August 31, 1997), $205,218 (with G. Papavassilopoulos. My share is one half of the grant.)

[11] NSF Grant No. MIP-9223812, “The USC Multiprocessor Testbed: A Testbed for Scalable Shared-Memory Multiprocessors,” from June 1993 to August 31 1996 (extended through August 31, 1997), $973,477 (no co-PI).

[12] NSF Grant No. MIP-9223812“Hardware Prototyping of Shared-Memory Multiprocessor Architectures on RPM,” from September 1996 to August 2000, $794,566 (no co-PI).

[13] HP Grant "Low-Cost Scalable Cache Coherent Shared-memory Systems", from January 1999 to May 1999, $15,000 (no co-PI)

[14] HP Grant,"Evaluation of Multi-engine Coherence Controllers with ILP Processors," from

September 1999 to May 2000, $18,000 (no co-PI)

[15] IBM Faculty Partnership Award:"Trace-driven Simlations of Commercial Workloads," from September 2001 to August 2002, $40,000 (no co-PI).

[16] NSF Grant No. CCR-0105761,"Trace Driven Evaluations of the Memory Behavior of Large Commercial Applications," from September 2001 to August 2004, $280,640 (no co-PI). No cost extension until August 2005.

[17] MECCA: Meeting Emerging Challenges in Comp. Architecture 9/01 to 12/06. STINT is a travel grant of $50,000/year renewable every year for 5 years. This is a Swedish state grant, obtained in collaboration with Per Stenstrom from Chalmers University, Goteborg to promote exchanges between Chalmers and USC. The grant is managed at Chalmers University.

[18] Xerox Corporation. "High-Performance Processors with Configurable Extended Instructions, from January 2005 to Januray 2008, $60,000 (no co-PI).

(2) Current

[19] NSF Grant No. CNS-0615428,"CSR-SMA: Collaborative Research-STAMP: A Universal Algorithmic Model for Next-Generation Multithreaded Machines" from August 2006 to July 2008, $150,000 (co-PI: Hyunyoung Lee, University of Denver).

F. Patent

United State Letters Patent #5,361,340. Title: “Apparatus for maintaining Consistency in a Multiprocessor Computer System Using Virtual Cacheing.” Inventors: Edmund Kelly, Michel Cekleov, and Michel Dubois, December 1994. This invention is a new method to maintain cache coherence on a multiprocessor bus using virtual addresses.

G. Graduated PhD Students

[1] Christoph Scheurich received his Ph.D. in May 1989. Thesis title: “Access Ordering and Coherence in Shared-Memory Multiprocessors”. Employment at the time of graduation: Intel Corp., Santa Clara, CA. Current employment: same.

[2] Aydin Uresin received his Ph.D. in April 1990. Thesis title: “Asynchronous iterations for Problems with Discrete Data.” Employment at the time of graduation: Assistant Professor, Istanbul Technical University, Istanbul, Turkey. .

[3] Jin-Chin Wang received his PhD in August 1990. Thesis title: “Analytical Modeling of Shared-Data Contention in Cache Coherence Protocols.” Employment at the time of graduation: IBM, Workstation Division, Austin, TX. Current employment: Sun Microsystems, Mountain View, CA.

[4] Fong Pong received his PhD in May 1995. Thesis title: “Symbolic State Model: A New Approach for the Verification of Cache Coherence Protocols”. Employment at the time of graduation: Sun Microsystems, Mountain View, CA. Current employment: HP Labs, Palo Alto, CA.

[5] Luiz Barroso graduated in September 1996. Thesis title: "Design Options for Small Scale Shared-Memory Multiprocessors". Employment at the time of graduation: DEC Western Research Laboratory, Palo Alto, CA.

[6] Kangwoo Lee graduated in December 1997. Thesis title:"Empirical Performance Modeling of Multiprocessors Based on Data-Sharing Analysis." Employment at the time of graduation: Assistant Professor, Dong-gook University, Seoul, Korea.

[7] Adrian Moga graduated in February 1998. Thesis title:"Design and Performance of the Software Controlled COMA." Employment at the time of graduation: Sequent Computers, Portland, Oregon.

[8] Xiaogang Qiu graduated in July 2000. Thesis title: "Towards Virtually-Addressed Memory Hierarchies," Employment at the time of graduation: Sun Microsystems, Sunnyvale, CA.

[9] Jaeheon Jeong graduated in May 2002. Thesis title: "Cost-sensitive Cache Replacement Algorithms," Employment at the time of graduation: IBM, Beaverton, OR.

H. Developed Artifacts

To support my research in computer architecture, I have developed, in the past 4 years and with the help of my graduate students, the following artifacts:

- A simulation environment to run parallel programs on simulated architectures. This is one of the most sophisticated environment available today in terms of the level of details at which hardware and software can be simulated.
- A CAD tool called SSM (Symbolic State Model) to help create complete verifications of coherence protocols based on Symbolic States (research with Fong Pong). This tool uses state expansion to explore and check all reachable system states. Thus it proves correctness of a protocol by exhaustive search. However, to avoid the complexity wall caused by the state space explosion problem, we represent states symbolically. This tool has been used by engineers at Intel and Cray Research.
- A multiprocessor emulator call RPM (Rapid Prototyping engine for Multiprocessors), built under NSF funding. RPM is a multiprocessor system which can be configured by modifying the programs of FPGAs (Field Programmable Arrays). This emulator is made of 10 boards connected to a backplane bus. The goal of the project is to demonstrate a new cost-effective methodology to validate architectures with low-cost hardware prototypes and to explore and compare the effectiveness of new ideas in multiprocessor architecture. This hardware took three years to develop.

I. Membership to Professional Societies

Michel Dubois is a member of the ACM and of the Computer Society of IEEE. He is an IEEE Fellow since 1999 and an ACM Fellow since 2005.

SERVICE

Professional (since 1990)

[1] Conferences

- Member (multiple times) of the program committees of the Int. Symposium on Computer Architecture (ISCA), of Mascott, of EURO-PAR, of the High-Performance Computer Architecture Symposium (HPCA), of the Int. Parallel Proc. Symposium (IPPS), of the IEEE Int. Conf on Distributed Computing Systems, of the Int. Conf. on Parallel Processing (ICPP), of the Symposium on Parallel Algorithms and Architectures (SPAA), of the Int. Conference on Supercomputing (ICS), of the Parallel Architecture and Compilation Techniques (PACT), of the International Conference on High-Performance Computing (Hi-PC).
- Vice Program Chair, 13th IEEE Int. Conf. on Distributed Computing Systems, 1993.
- Program Chair, High-Performance Computer Architecture Symposium (HPCA), 1996.
- Program Chair, International Symposium on Computer Architecture (ISCA), 2001.
- General Chair, International Symposium on Computer Architecture (ISCA), 2004.
- Program co-Chair, ACM/IEEE Symposium on Architectures for Networking and Communications Systems (ANCS), 2006
- Program co-Chair, Computing Frontiers 2007.
- General co-Chair, HiPeac Conference, 2007

[2] Journals

- Guest Editor for a special issue of IEEE Computer on cache-based multiprocessors, which appeared in June 1990 (with S. Thakkar).
- Guest Editor for a special issue of the Journal of Parallel and Distributed Computing (JPDC) on “Memory System Architectures for Scalable Multiprocessors” August 1992 (with S. Thakkar).
- Reviewer for numerous papers for IEEE Transactions, Journal of the ACM, IEEE Computer, Journal of Parallel and Distributed Computing, Journal of Parallel Computing and much more...
- Area Editor for the Journal of Parallel and Distributed Computing (JPDC).
- Associate Editor for the IEEE Transactions on Computers (IEEE-TC).

[3] Workshops

- Organizer of the workshop on “Cache and Interconnect Architectures in Multiprocessors,” at the 1989 Symposium on Computer Architecture at Eilat, Israel, May 1989. Editor of the Proceedings for this workshop, which appeared in June 1990 (Kluwer) (with S. Thakkar).
- Organizer of the workshop on “Scalable Shared-memory Multiprocessors,” at the 1990 Symposium on Computer Architecture at Seattle, Washington, May 1990. Editor of the Proceedings for this workshop, published by Kluwer (with S. Thakkar).
- Organizer of the Workshop on Scalable Shared-memory Multiprocessors, in 1992, 1993, 1994, 1995, and 1996 (with S. Thakkar). (no proceedings) This is a very popular workshop

regularly attracting more than 75 participants each year.

[4] Conference Panels.

- At ISCA'93 "To Cache or not to Cache" with Zary Segall (CMU), John Hennessy (Stanford) and Burton Smith (Tera)
- At HPCA'95 "How can we avoid that computer architecture becomes the science of irreproducible results." with Trevor Mudge (Michigan), James Goodman (Wisconsin), Tilak Agerwala (IBM), and Michael Foster (NSF).
- At HPCA'96 "To build or not to build: Perils of architecture research in academia," with Arvind (MIT), Anant Agarwal (MIT), Anoop Gupta (Stanford), Jean-Loup Baer (Washington), David Culler (Berkeley), Trevor Mudge (Michigan) and David Wood (Wisconsin).
- At IPDPS 07: "Is the Multi-Core Roadmap going to Live Up to its Promises?" with Per Stenstrom (Chalmers), Tim Mattson (Intel), Kunle Olukotun (Stanford), David Padua (UIUC) and Marc Tremblay (Sun Microsystems).

[5] National Science Foundation Conference. Participated in the "NSF Conference on Experimental Research In Computer Science", held in Washington DC in June 1996. This conference will review several experimental projects supported by NSF, assess the current state of experimental computer science research, and identify future opportunities.

[6] NSF: CAREER AWARD PANELS

[7] NSF PANELS on Computer Architecture.

[8] Nominated and selected to be part of the ACM/IEEE Eckert-Mauchly award selection committee. This is a committee of six who receive nominations for the Eckert-Mauchly award, the most prestigious award in the field of Computer Architecture, and select the recipient among nominated individuals. 2001-2003: Committee Member. 2004 : Committee Chair.

[9] IEEE Computer Society TCCA committee 2006-